CCD486
4k x 4k Image Area
Full Frame CCD Image Sensor

FEATURES
- **4096(H) x 4097(V) Full Frame CCD Array**
- **15 µm x 15 µm Pixel**
- **61.44 mm x 61.455 mm Image Area**
- **100% Fill Factor**
- **Available in Front and Back Illuminated Formats**
- **Multi-Pinned Phase (MPP) Operation**
- **Readout Noise Less Than 5 e^- at 50k pixels/sec**
- **Dynamic Range Better Than 86 dB in MPP**
- **Four Low Noise Output Amplifiers**
- **Three Phase Buried Channel CCD**
- **Supports Pixel Binning**

GENERAL DESCRIPTION

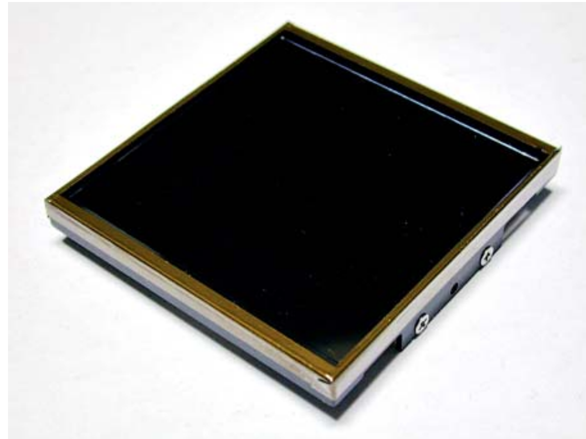
The CCD486 is a 4096(H) x 4097(V) pixels solid state Charge Coupled Device (CCD) Full Frame sensor. The CCD is intended for advanced scientific, space, industrial, and commercial digital imaging applications. The CCD486 is organized as an array of 4096 horizontal by 4097 vertical imaging elements. The pixel pitch is 15µm with a 100% fill factor. For dark reference, each readout line is preceded by 18 dark pixels. The imager is available in front-illuminated as well as back-illuminated configuration (as shown in photo at right). A split readout architecture has been adopted to accommodate high data rates with simultaneous readout out of four output ports, or reduced data rates using two output ports, or readout of the entire image frame from a single output port in order to simplify the drive electronics requirements.

A single-stage source follower output amplifier design was chosen for low noise performance. The readout noise floor is typically better than 5 e^- at a pixel rate of 50 kHz. Each output amplifier is capable of operating at up to 1 MHz with less than 10 e^- nominal read noise.

The CCD486 is mounted in ceramic packages for improved flatness uniformity. Frontside devices are mounted in 71mm x 71mm (2.8" x 2.8") PGA packages. Back-illuminated devices are mounted in 61mm x 64mm (2.4" x 2.5") PGA packages, and a metal frame is attached to the headers to support a glass protection window. Both packages have 54 pins.

Pin Number / Name

1. GND-UR	17. ΦSG-UL	33. ΦR-LL	49. ΦR-LR
2. V1-UR	18. VOG-UL	34. VRD-LL	50. VTG-LR
3. V2-UR	19. VOUT-UL	35. VDD-LL	51. V3-L
4. V3-U	20. VDD-UL	36. VOUT-LL	52. V2-LR
5. VTG-UR	21. VRD-UL	37. VOG-LL	53. V1-LR
6. ΦR-UR	22. ΦR-UL	38. ΦSG-LL	54. GND-LR
7. VRD-UR	23. VTG-UL	39. H1-LL	
8. VDD-UR	24. V3-U	40. H2-LL	
9. VOUT-UR	25. V2-UL	41. H3-L	
10. VOG-UR	26. V1-UL	42. H2-LR	
11. ΦSG-UR	27. GND-UL	43. H1-LR	
12. H1-UR	28. GND-LL	44. ΦSG-LR	
13. H2-UR	29. V1-LL	45. VOG-LR	
14. H3-U	30. V2-LL	46. VOUT-LR	
15. H2-UL	31. V3-L	47. VDD-LR	
16. H1-UL	32. VTG-LL	48. VRD-LR	



Back-illuminated CCD486 in ceramic header

FUNCTIONAL DESCRIPTION

The following functional elements are illustrated in the block diagram:

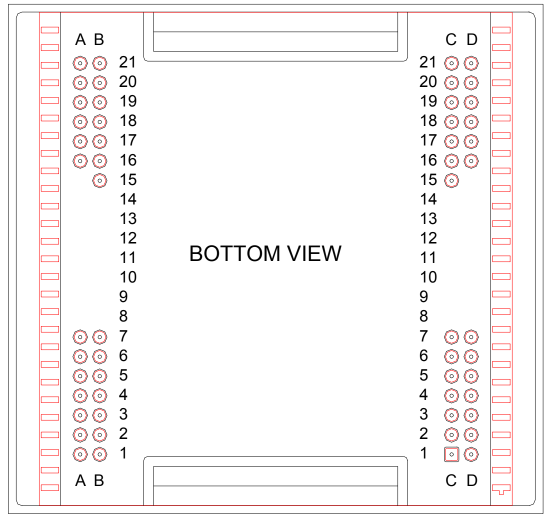
Image Sensing Elements: In frontside illumination mode, incident photons pass through a transparent polycrystalline silicon gate structure creating electron hole pairs. The resulting photoelectrons are collected in the photosites during the integration period. The amount of charge accumulated in each photosite is a linear function of the localized incident illumination intensity and integration period.

In the backside illuminated mode, incident photons are collected on the backside of the CCD which has been thinned to about 18 microns. An accumulated surface potential helps direct the generated charge to the CCD depletion wells and is accomplished by applying a special surface treatment to the backside. The backside antireflection coatings can be tailored to optimize the device sensitivity over a range of spectral bands.

Pin Number / Name

C1. GND-UR	C16. ΦSG-UL	A19. ΦR-LL	A3. ΦR-LR
D1. V1-UR	D17. VOG-UL	B18. VRD-LL	B3. VTG-LR
C2. V2-UR	C17. VOUT-UL	A18. VDD-LL	A2. V3-L
D2. V3-U	D18. VDD-UL	B17. VOUT-LL	B2. V2-LR
C3. VTG-UR	C18. VRD-UL	A17. VOG-LL	A1. V1-LR
D3. ΦR-UR	D19. ΦR-UL	B16. ΦSG-LL	B1. GND-LR
C4. VRD-UR	C19. VTG-UL	A16. H1-LL	
D4. VDD-UR	D20. V3-U	B15. H2-LL	
C5. VOUT-UR	C20. V2-UL	A7. H3-L	
D5. VOG-UR	D21. V1-UL	B7. H2-LR	
C6. ΦSG-UR	C21. GND-UL	A6. H1-LR	
D6. H1-UR	B21. GND-LL	B6. ΦSG-LR	
C7. H2-UR	A21. V1-LL	A5. VOG-LR	
D7. H3-U	B20. V2-LL	B5. VOUT-LR	
C15. H2-UL	A20. V3-L	A4. VDD-LR	
D16. H1-UL	B19. VTG-LL	B4. VRD-LR	

BACK-ILLUMINATED CCD486
HEADER WITH ATTACHED
WINDOW FRAME



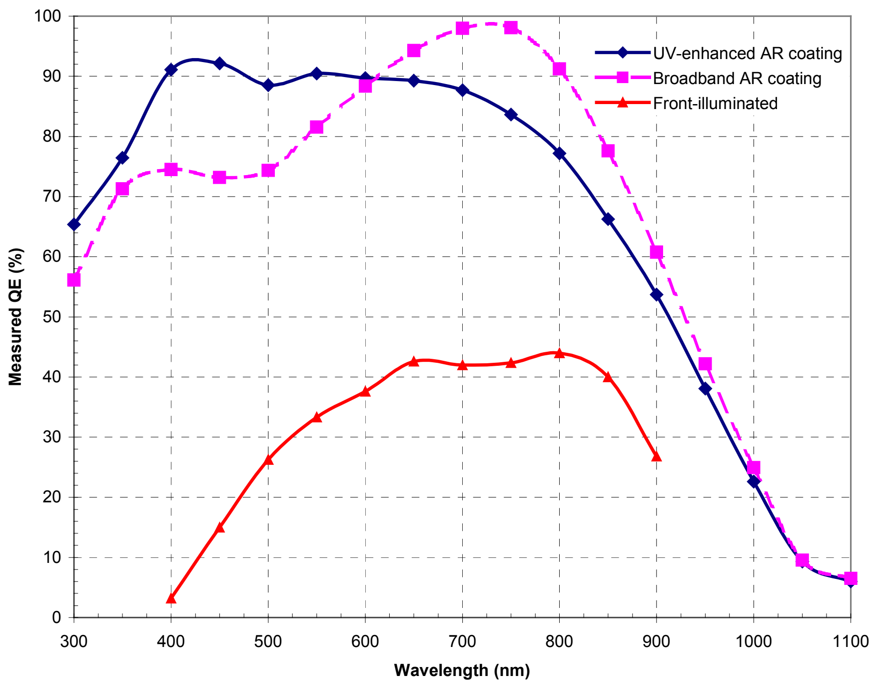
The photosite structure is made up of contiguous CCD elements with no voids or inactive areas. In addition to sensing light, these elements are used to shift image charge vertically. Consequently, the device needs to be mechanically shuttered during readout.

Vertical Charge Shifting: The architecture of the CCD486 provides video information as a single sequential readout of 4097 lines containing 4096 photosensitive elements. At the end of an integration period the ΦV_1, ΦV_2, and ΦV_3 clocks are used to transfer charge vertically through the CCD array to the horizontal readout register. Vertical columns are separated by channel stop regions to confine charge laterally. The Vertical Transfer Gate (ΦVTG) is the final array gate before charge is transferred to the serial horizontal shift registers. For simplified operation ΦVTG may be tied to ΦV_3.

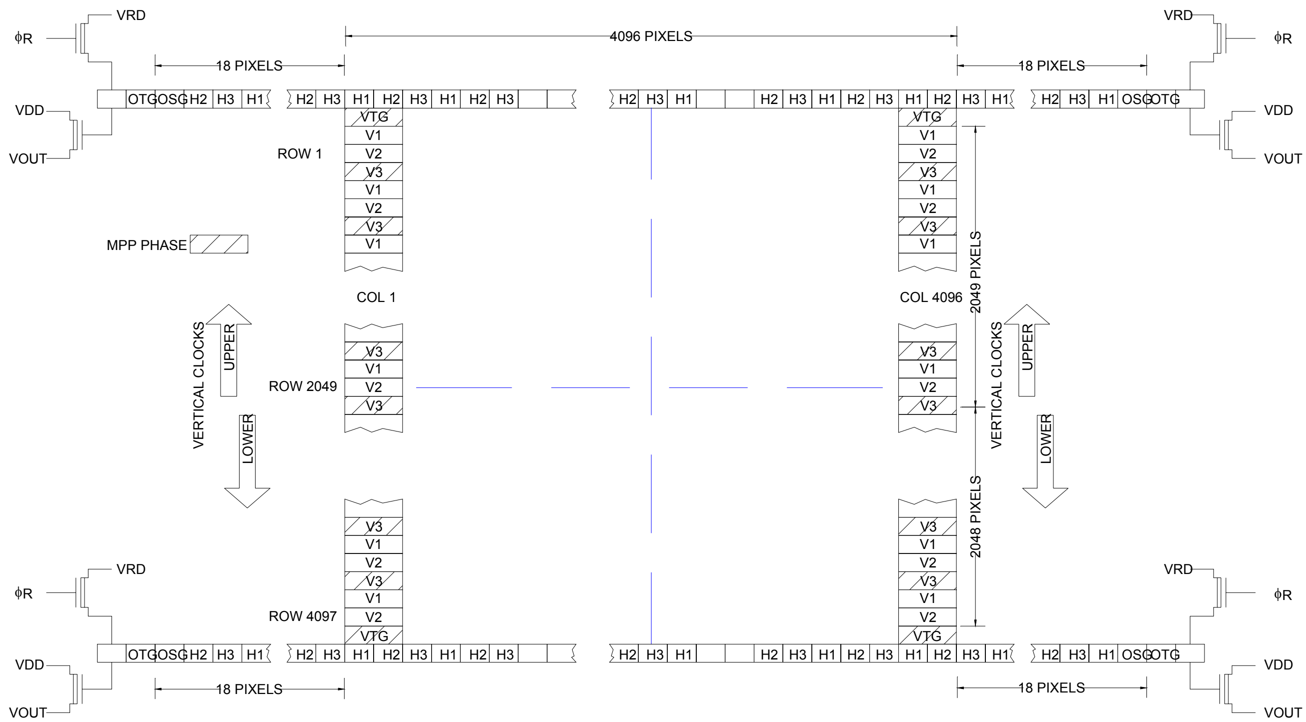
The imaging area is electrically divided into four quadrants. Each 2048 x 2048 segment may be clocked independently or combined as required. Horizontal serial registers along the top and bottom permit simultaneous readout of the upper and lower halves. The CCD486 also may be clocked such that the full array is read out through the Upper or the Lower serial registers.

Horizontal Charge Shifting: ΦH_1, ΦH_2, and ΦH_3 are polysilicon gates used to transfer charge horizontally to the output amplifier. The horizontal transport register is twice the size of the photosite to allow for vertical binning, and a summing well is provided to support horizontal binning. The array can be read out normally at 4k(H) x 4k(V) full resolution, as a 4k(H) x 2k(V), or 2k(H) x 2k(V). The horizontal shift registers are bi-directional so that the image

Quantum Efficiency



CCD486 FUNCTIONAL DIAGRAM



frame may be read out through a single, or two amplifiers per serial register.

The transfer of charge into the horizontal register is the result of a vertical shift sequence. This register has 18 additional register cells between the first pixel of each line and the output amplifier. The output from these locations contains no signal and may be used as a dark level reference.

The last clocked gate in the Horizontal registers is twice as large as the others and can be used to combine the signal charge of the pixels in the horizontal shift registers. This gate requires its own clock, which may be tied to ΦH_1 for normal full resolution readout. The output video is available following the High to Low transition of ΦSG.

The reset FET in the horizontal readout, clocked appropriately with ΦR, allows binning of adjacent pixels.

Output Amplifier: The CCD486 has an output amplifier at each end of the horizontal shift registers for a total of four output ports. The single-stage amplifier design has been optimized for low readout noise. Signal charge packets are serially clocked to a pre-charged capacitor, the sense node, whose potential changes linearly in response to the number of electrons delivered. This potential is applied to the input gate of an NMOS amplifier producing a signal at the output V_{out} pin. The capacitor is reset with ΦR to a pre-charge level prior to the arrival of the next charge packet (except when horizontal binning is performed). It is reset by use of the reset MOSFET. The output amplifier drain is tied to VDD. The source is connected to an external load resistor to ground. The voltage change at the source constitutes the video output from the device.

Multi-Pinned Phase: MPP is a CCD technology which significantly reduces the dark current generation rate. CCDs are endowed with this capability by the addition of an ion implant step during the semiconductor manufacturing process.

This implant creates a built-in potential barrier in each pixel, which allows charge integration to be performed with all of the vertical clocks biased at their Low levels (-8V). Under these conditions, the surface potential of the CCD is pinned at 0V, and the holes released by the neighboring p+ channel stops recombine with the electrons that are generated by surface defects which effectively neutralize the surface dark current.

A drawback in operating in MPP mode is the reduced full well capacity. The potential barrier created by MPP implant does not hold as much charge as the normal buried channel operating mode which stores charge under one of the vertical gates biased High during integration. The CCD486 fabrication process has been optimized to maximize the charge capacity in MPP mode.

DEFINITION OF TERMS

Charge-Coupled Device: A charge-coupled device is a monolithic silicon structure in which discrete packets of electron charge are transported from position to position by sequential clocking of an array of gates.

Vertical Transport Clocks ΦV_1, ΦV_2, ΦV_3: The clock signals applied to the vertical transport register.

Vertical Transfer Gate ΦVTG: Gate structures adjacent to the end row of photosites and the horizontal transport registers. The charge packets accumulated in the photosites are shifted vertically through the array. Upon reaching the last row of photosites, the charge is transferred in parallel via the vertical transfer gate to the horizontal transport shift registers when the transfer gate clock voltage goes low.

Horizontal Transport Clocks ΦH_1, ΦH_2, ΦH_3: The clock signals applied to the horizontal transport registers.

Reset Clock ΦR: The clock applied to the reset switch of the output amplifier.

Dynamic Range: The ratio of saturation output voltage to RMS noise in the dark. The peak-to-peak random noise is 4-6 times the RMS noise output.

Saturation Exposure: The minimum exposure level that produces an output signal corresponding to the maximum photosite charge capacity. Exposure is equal to the product of light intensity and integration time.

Responsivity: The output signal voltage per unit of exposure.

Spectral Response Range: The spectral band over which the response per unit of radiant power is more than 10% of the peak response.

Photo-Response Non-Uniformity: The difference of the response levels between the most and the least sensitive regions under uniform illumination (excluding blemished elements) expressed as a percentage of the average response.

Dark Signal: The output signal in the caused by thermally generated electrons. Dark signal is a linear function of integration time, and varies exponentially as a function of the chip temperature.

Pixel: Picture element or sensor element (also called photoelement or photosite).

DEVICE HANDLING PRECAUTIONS

Due to the negative bias conditions necessary for proper operation, the CCD486 is not equipped with built-in ESD protection circuitry. Strict ESD procedures and proper handling precautions must be performed to avoid accidental damage to the devices. The warranty does not apply to ESD damaged devices.

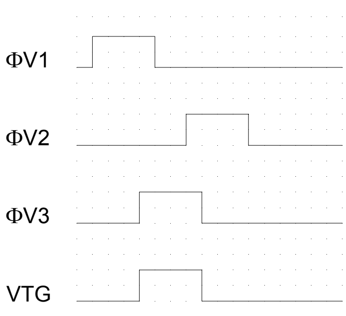
- Always store the devices with the shorting pins that are shipped with the devices securely attached to all of the pins.
- Never insert or remove the device from a live socket or operating camera. Turn-off all electrical power first.
- Test stations must be specifically designed to minimize static charge build-up, including ionizing air blowers, and grounded floor mats.
- The relative humidity level in the working environment must be controlled between 40% - 60%.
- Never handle the devices without proper personal ESD protection items such as tested grounding straps, electrically conductive gloves or finger cots, ESD safe smocks, conductive shoe straps are also desirable.

ABSOLUTE MAXIMUM RATINGS

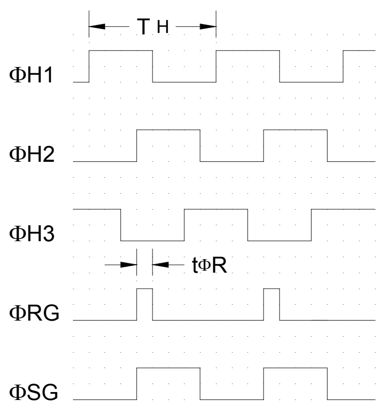
Storage temperature range .... -50 ºC to +75 ºC
Operating temperature range .... -90 ºC to +40 ºC

TIMING DIAGRAMS

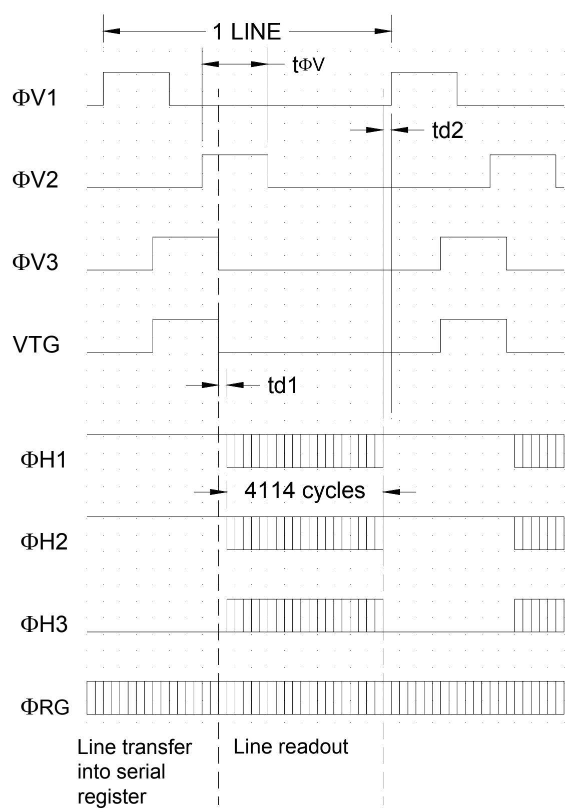
VERTICAL TIMING (SHIFT UP)



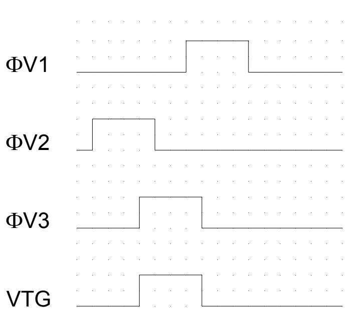
PIXEL TIMING (SHIFT RIGHT)



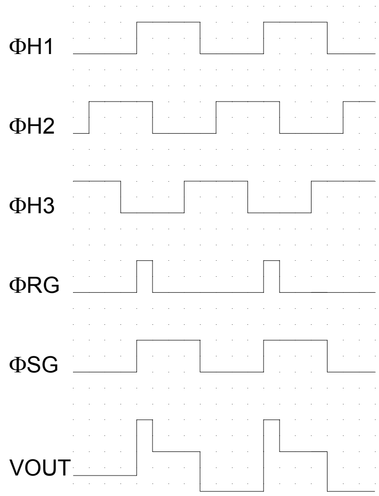
LINE TIMING



VERTICAL TIMING (SHIFT DOWN)



PIXEL TIMING (SHIFT LEFT)



TYPICAL TIMING PARAMETERS

PARAMETER		SYMBOL	VALUE	UNIT	REMARKS
Horizontal clock frequency		f_H	400	kHz	
Horizontal clock pulse width		tΦH	1.25	μs	
Horizontal clock overlap		f_H-ovl	0.3	μs	
Horizontal blanking time		H-blank	600	μs	
Vertical clock frequency		f_V	2.5	kHz	
Vertical clock pulse width	V1, V2 V3	tΦV1, tΦV2 tΦV3	200 300	μs μs	
Vertical clock rise and fall times		ΦVtr, ΦVtf	200	ns	
Vertical clock overlap		f_V-ovl	26	μs	
Reset clock pulse width		tΦR	300	ns	

GENERAL INFORMATION

PARAMETER		**Front-illuminated**	**Back-illuminated**	UNIT	REMARKS
Active pixels	Horizontal Vertical	4096 4097	4096 4037		
Pixel size		15 x 15	15 x 15	μm^2	
Active image area		61.440 x 61.455	61.440 x 60.555	mm^2	
Number of prescan pixels		18	18		
Number of output amplifiers		4	4		

DC OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT	REMARKS
V_{DD}	DC Supply Voltage	18	27	28	V	
V_{RD}	Reset Drain Voltage	13	17	18	V	
V_{OG}	Output Gate Voltage	- 5	-2.5	1	V	
V_{SS}	Substrate Ground	0	0	0	V	

TYPICAL CLOCK VOLTAGES

SYMBOL	PARAMETER	HIGH	LOW	UNIT	REMARKS
$V\Phi_{H(1,2,3)}$	Horizontal Register Clocks	+5	-5	V	
$V\Phi_{SG}$	Summing Gate Clock	+5	-5	V	
$V\Phi_{V(1,2)}$	Vertical Register Clock	+3	-8	V	
$V\Phi_{V(3)}$	Vertical Register Clock	+4.5	-6	V	
$V\Phi_R$	Reset Clock	+8	0	V	
$V\Phi_{VTG}$	Array Transfer Gate Clock	+4.5	-6	V	

AC CHARACTERISTICS Standard test conditions are: 23 ºC, nominal MPP clocks, and DC operating voltages, 400 kHz Horizontal clock frequency, 2.5 kHz Vertical clock frequency

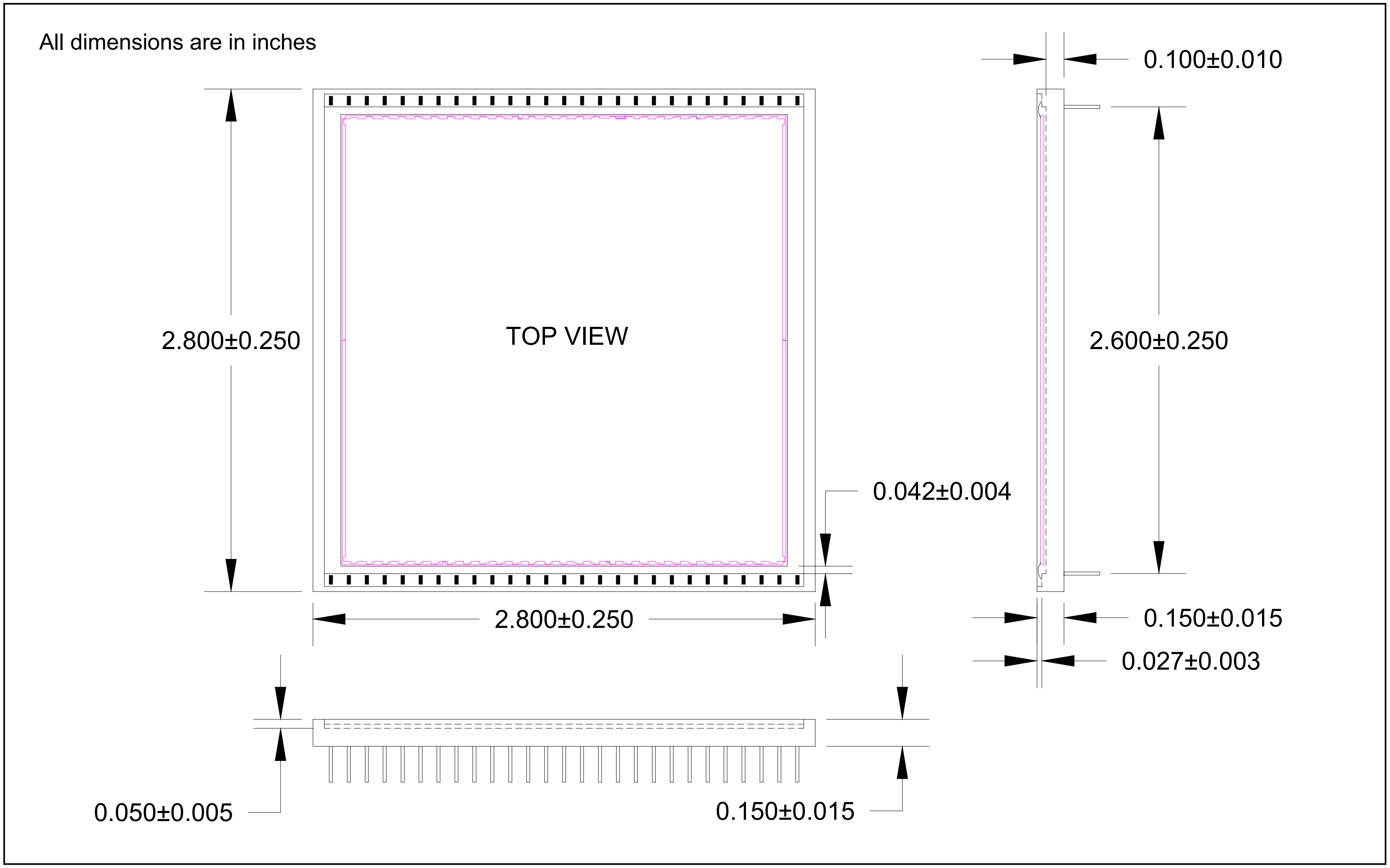
SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT	REMARKS
Z	Suggested Load Resistor	5	10	20	KΩ	

PERFORMANCE SPECIFICATIONS

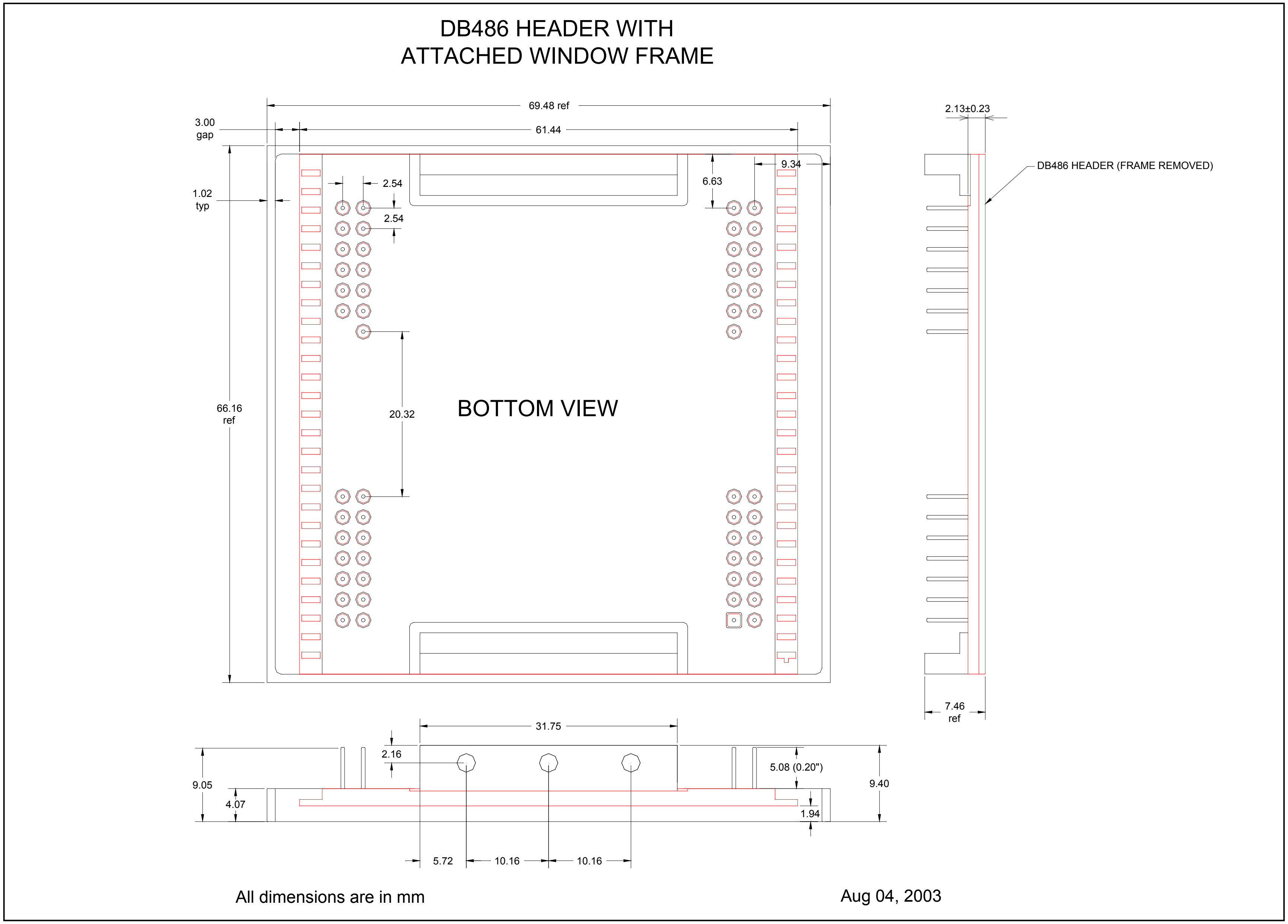
SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT	REMARKS
F read	Readout frequency		400	1000	kHz	
N read	Readout noise		12	16	e- per pix	
V_{SAT}	Saturation Output Voltage	136	300		mV	
FW (V)	Vertical Register Full Well Capacity	85	100		ke-	
FW (H)	Horizontal Register Full Well Capacity	650	750		ke-	
Nsat	Output Node Charge Capacity	700	800		ke-	
OCG	Output Amplifier Conversion Gain	1.6	3		μV/e-	
PRNU	Photo Response Non-Uniformity			10	% V_{SAT}	Measured at half saturation
DC	Dark Current (MPP)		25	50	pA/cm^2	Note 1
DSNU	Dark Current Non Uniformity		25	50	pA/cm^2	Peak-to-peak
R	Peak Responsivity		5		$V/\mu J/cm^2$	Frontside illuminated

Note 1: Values shown are at 25°C. Dark current doubles for every 7°C

PACKAGE INFORMATION



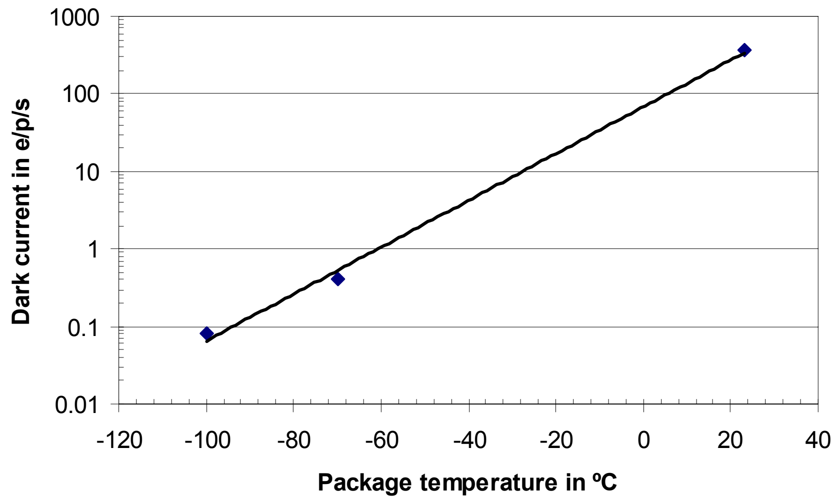
Mechanical drawing of the PGA package of the front-illuminated CCD486



Mechanical drawing of the PGA package of the back-illuminated CCD486

DARK CURRENT CHARACTERISTICS

CCD486 FI
Typical change in dark current with temperature



BLEMISH SPECIFICATIONS
The CCD486 is available in several different cosmetic grades, as shown below. Custom selected grades are also available. Consult your Sales representative for custom grade requirements.

		Blemish Specification			
		Total Array			
Product	**Grade**	**Point Defects**	**Column Defects Total**	**Column Defects Adjacent**	**Clusters Defects**
CCD486	1	200	5	2	25
4096 x 4096 CCD	2	400	10	3	50
15-um pixels	3	800	>10	>3	100

Defect exclusion zone: Defect measurements are excluded from the outer two rows and columns of the sensor

Cosmetic Defect Specifications	
Point Defect	**Dark pixel:** A pixel which amplitude is below 50% of the mean signal tested at 85 ke^- **Hot pixel:** A pixel which generates more than $10e^-$/pixel/sec at –40C
Cluster Defect	A grouping of 9 adjacent point defects or less (excluding the pixels in colum defects)
Column Defect	A grouping of more than 10 contiguous point defects in a single column

WARRANTY
Within twelve months of delivery to the original customer, Fairchild Imaging will repair or replace, at our option, any Fairchild Imaging components, or camera products, if any part is found to be defective in materials or workmanship. Contact Customer Service for assignment of warranty return number and shipping instructions to ensure prompt repair or replacement.

CERTIFICATION
Fairchild Imaging certifies that its products are fully inspected and tested at the factory prior to shipment, and that they conform to the stated specifications. This product is designed, manufactured, and distributed utilizing the ISO 9000:2000 Business Management System.

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